Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Claims 1-163 (Cancelled).

164. (Cancelled)

165. (Currently Amended) The CMOS integrated circuit of claim ~~164~~ 298 wherein the tunable oscillator comprises a voltage controlled oscillator.

166. (Currently Amended) The CMOS integrated circuit of claim ~~164~~ 298 wherein the transmitter further comprises a bandpass filter coupled between the mixer output and the first input of the phase detector.

167. (Previously Presented) The CMOS integrated circuit of claim 166 wherein the transmitter further comprises a limiter coupled between the bandpass filter and the first input of the phase detector.

168. (Currently Amended) The CMOS integrated circuit of claim ~~164~~ 298 wherein the transmitter further comprises a charge pump coupled between the phase detector output and the tuning input.

169. (Currently Amended) The CMOS integrated circuit of claim ~~164~~ 298 wherein the transmitter further comprises a loop filter coupled between the phase detector output and the tuning input.

170. (Currently Amended) The CMOS integrated circuit of claim ~~164~~ 298 wherein the tunable oscillator comprises a voltage controlled oscillator, the CMOS integrated circuit further comprising a bandpass filter coupled to the mixer, a limiter coupled between the bandpass filter and the first input of the phase detector, a charge pump coupled to the phase detector output, and a loop filter coupled between the charge pump and the tuning input.

171. (Currently Amended) The CMOS integrated circuit of claim ~~164~~ 298 wherein the mixer comprises a subsampling mixer.

172. (Previously Presented) The CMOS integrated circuit of claim 171 wherein the mixer comprises a track and hold circuit coupled to the inputs of the mixer and the output of the mixer, and a bandpass circuit coupled to the first input of the mixer and the output of the mixer.

173. (Previously Presented) The CMOS integrated circuit of claim 172 wherein the mixer further comprises an input circuit disposed between the first input of the mixer and the track and hold circuit.

174. (Previously Presented) The CMOS integrated circuit of claim 172 wherein the mixer further comprises a buffer disposed between the track and hold circuit and the output of the mixer.

175. (Previously Presented) The CMOS integrated circuit of claim 172 wherein the bandpass circuit comprises an inductor coupled to the first input of the mixer and a capacitor coupled to the output of the mixer.

176. (Previously Presented) The CMOS integrated circuit of claim 172 wherein the track and hold circuit comprises a switch between the first input of the mixer and the output of the mixer, the switch being adapted for control by a signal applied to the second input of the mixer from the local oscillator.

177. (Previously Presented) The CMOS integrated circuit of claim 176 wherein the switch comprises a transistor having a gate coupled to the second input of the mixer, a source coupled to the first input of the mixer, and a drain, and wherein the bandpass circuit comprises a capacitor coupled to the drain, and an inductor coupled to the source.

178. (Previously Presented) The CMOS integrated circuit of claim 177 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the first input of the mixer from the tunable oscillator.

179. (Previously Presented) The CMOS integrated circuit of claim 172 wherein the track and hold circuit comprises a transistor having an input node coupled to the first input of the mixer and an output node coupled to the output of the mixer, and a current source coupled to the output of the mixer, the current source being adapted for control by a signal applied to the second input of the mixer.

180. (Previously Presented) The CMOS integrated circuit of claim 179 wherein the current source comprises a second transistor having a gate coupled to the first input of the mixer, a drain coupled to the output of the mixer, and a source, and wherein the bandpass circuit comprises a capacitor coupled to the output of the mixer and an inductor coupled to the drain of the second transistor.

181. (Previously Presented) The CMOS integrated circuit of claim 180 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the first input of the mixer from the tunable oscillator.

182. (Cancelled)

183. (Currently Amended) The transmission system of claim ~~182~~ 299 wherein the tunable oscillator comprises a voltage controlled oscillator.

184. (Currently Amended) The transmission system of claim ~~182~~ 299 wherein the transmitter further comprises a bandpass filter coupled between the subsampling mixer output and the first input of the phase detector.

185. (Previously Presented) The transmission system of claim 184 wherein the transmitter further comprises a limiter coupled between the bandpass filter and the first input of the phase detector.

186. (Currently Amended) The transmission system of claim ~~182~~ 299 wherein the transmitter further comprises a charge pump coupled between the phase detector output and the tuning input.

187. (Currently Amended) The transmission system of claim ~~182~~ 299 wherein the transmitter further comprises a loop filter coupled between the phase detector output and the tuning input.

188. (Currently Amended) The transmission system of claim ~~182~~ 299 wherein the tunable oscillator comprises a voltage controlled oscillator, the transmission system further comprising a bandpass filter coupled to the mixer output, a limiter coupled between the bandpass filter and the first input of the phase detector, a charge pump coupled to the phase detector output, and a loop filter coupled between the charge pump and the tuning input.

189. (Previously Presented) The transmission system of claim 171 wherein the mixer comprises a track and hold circuit coupled to the inputs of the mixer and the output of the mixer, and a bandpass circuit coupled to the first input of the mixer and the output of the mixer.

190. (Previously Presented) The transmission system of claim 189 wherein the mixer further comprises an input circuit disposed between the first input of the mixer and the track and hold circuit.

191. (Previously Presented) The transmission system of claim 189 wherein the mixer further comprises a buffer disposed between the track and hold circuit and the output of the mixer.

192. (Previously Presented) The transmission system of claim 189 wherein the bandpass circuit comprises an inductor coupled to the first input of the mixer and a capacitor coupled to the output of the mixer.

193. (Previously Presented) The transmission system of claim 189 wherein the track and hold circuit comprises a switch between the first input of the mixer and the output of the mixer, the switch being adapted for control by a signal applied to the second input of the mixer from the local oscillator.

194. (Previously Presented) The transmission system of claim 193 wherein the switch comprises a transistor having a gate coupled to the second input of the mixer, a source coupled to the first input of the mixer, and a drain, and wherein the bandpass circuit comprises a capacitor coupled to the drain, and an inductor coupled to the source.

195. (Previously Presented) The transmission system of claim 194 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the first input of the mixer from the tunable oscillator.

196. (Previously Presented) The transmission system of claim 189 wherein the track and hold circuit comprises a transistor having an input node coupled to the first input of the mixer and an output node coupled to the output of the mixer, and a current source coupled to the output of the mixer, the current source being adapted for control by a signal applied to the second input of the mixer.

197. (Previously Presented) The transmission system of claim 196 wherein the current source comprises a second transistor having a gate coupled to the first input of the mixer, a drain coupled to the output of the mixer, and a source, and wherein the bandpass circuit comprises a capacitor coupled to the output of the mixer and an inductor coupled to the drain of the second transistor

198. (Previously Presented) The transmission system of claim 197 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the first input of the mixer from the tunable oscillator.

199. (Previously Presented) A complementary metal oxide semiconductor (CMOS) transmitter system, comprising:

first oscillator means for generating a first signal having a tunable frequency, the first oscillating means comprising tuning means for tuning the frequency of the first signal;

mixer means for mixing the first signal with a second signal to produce a mixed signal;

detector means for detecting a phase difference between the mixed signal and an input signal, and generating an error signal which is a function of the phase difference, the tuning means being responsive to the error signal; and

second oscillator means for generating the second signal.

200. (Previously Presented) The CMOS transmitter system of claim 199 wherein the first oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal.

201. (Previously Presented) The CMOS transmitter system of claim 199 further comprising filter means for filtering the mixed signal before being applied to the detector means, the filtered mixed signal comprising a difference frequency between the tuned frequency of the first signal and a frequency of the second signal.

202. (Previously Presented) The CMOS transmitter system of claim 201 further comprising means for limiting the filtered mixed signal from the filter means before being applied to the detector means.

203. (Previously Presented) The CMOS transmitter system of claim 199 further comprising means for sourcing current to the tuning means responsive to the error signal.

204. (Previously Presented) The CMOS transmitter system of claim 199 further comprising means for filtering the error signal from the detecting means before being applied to the tuning means.

205. (Previously Presented) The CMOS transmitter system of claim 199 wherein the first oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal, the CMOS transmitter system further comprising filter means for filtering the mixed signal before being applied to the detector means, the filtered mixed signal comprising a difference frequency between the tuned frequency of the first signal and a frequency of the second signal, means for limiting the filtered mixed signal from the filter means before being applied to the detector means, current means for sourcing current to the tuning means responsive to the error signal, and means for filtering the current sourced error signal from the current means before being applied to the tuning means.

206. (Previously Presented) The CMOS integrated circuit of claim 199 wherein the mixer means comprises a subsampling mixer.

207. (Previously Presented) The CMOS integrated circuit of claim 206 wherein the subsampling mixer comprises track and hold means for tracking and holding the first signal in response to the second signal, and limiting means for limiting the response of the track and hold means to a frequency band, the first signal being within the frequency band.

208. (Previously Presented) The CMOS integrated circuit of claim 207 further comprising means for buffering first signal before being applied to the track and hold means.

209. (Previously Presented) The CMOS integrated circuit of claim 207 wherein the limiting means comprises an inductor and capacitor each being coupled to the track and hold means.

210. (Previously Presented) The CMOS integrated circuit of claim 207 wherein the track and hold means comprises a switch in a path of the first signal, the switch being controlled by the second signal.

211. (Currently Amended) A transmitter system, comprising:

first oscillator means for generating a first signal having a tunable frequency, the first oscillating means comprising tuning means for tuning the frequency of the first signal;

mixer means for mixing the first signal with a second signal to produce a mixed signal;

filter means for filtering the mixed signal to generate a difference signal between the frequency of the first signal and a harmonic of the second signal; ~~and~~

detector means for detecting a phase difference between the filtered mixed signal and an input signal, and generating an error signal which is a function of the phase difference, the tuning means being responsive to the error signal; and

second oscillator means for generating the second signal.

212. (Previously Presented) The transmitter system of claim 211 wherein the first oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal.

213. (Previously Presented) The transmitter system of claim 211 wherein the second signal comprises a frequency different from the frequency of the first oscillator means

214. (Previously Presented) The transmitter system of claim 211 further comprising means for limiting the filtered mixed signal from the filter means before being applied to the detector means.

215. (Previously Presented) The transmitter system of claim 211 further comprising means for sourcing current to the tuning means responsive to the error signal.

216. (Previously Presented) The transmitter system of claim 211 further comprising means for filtering the error signal from the detecting means before being applied to the tuning means.

217. (Previously Presented) The transmitter system of claim 211 wherein the first oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal, and the second signal comprises a frequency different from the frequency of the first oscillator means, the transmitter system further comprising means for limiting the filtered mixed signal from the filter means before being applied to the detector means, current means for sourcing current to the tuning means responsive to the error signal, and means for filtering the current sourced error signal from the current means before being applied to the tuning means.

218. (Previously Presented) The transmitter system of claim 211 wherein the mixer comprises track and hold means for tracking and holding the first signal in response to the second signal, and limiting means for limiting the response of the track and hold means to a frequency band, the first signal being within the frequency band.

219. (Previously Presented) The transmitter system of claim 218 further comprising means for buffering first signal before being applied to the track and hold means

220. (Previously Presented) The transmitter system of claim 218 wherein the limiting means comprises an inductor and capacitor each being coupled to the track and hold means.

221. (Previously Presented) The transmitter system of claim 218 wherein the track and hold means comprises a switch in a path of the first signal, the switch being controlled by the second signal.

222. (Previously Presented) A spread spectrum wireless communications device, comprising:

an integrated circuit that employs complementary metal oxide semiconductor (CMOS) technology, the integrated circuit comprising a local oscillator and a transmitter,

wherein the transmitter comprises a tunable oscillator, a mixer and a phase detector,

wherein the tunable oscillator comprises a tuning input,

wherein the mixer comprises a first input, a second input and an output, the first input of the mixer being operatively coupled to the tunable oscillator,

wherein the phase detector comprises a first input, a second input and an output, the first input of the phase detector being operatively coupled to the output of the mixer, the output of the phase detector being operatively coupled to the tuning input, and

wherein the local oscillator is operatively coupled to the second input of the mixer.

223. (Previously Presented) The spread spectrum wireless communications device according to claim 222, wherein the integrated circuit is part of a single integrated circuit chip.

224. (Previously Presented) The spread spectrum communications device according to claim 222, wherein the spread spectrum communications device comprises a radio frequency (RF) wireless communications device.

225. (Previously Presented) The spread spectrum communications device according to claim 224, wherein the RF wireless communications device performs spread spectrum modulation.

226. (Previously Presented) The spread spectrum communications device according to claim 224, wherein the RF wireless communications device performs direct sequence spread spectrum modulation.

227. (Previously Presented) The spread spectrum communications device according to claim 226, wherein the RF wireless communications device performs orthogonal frequency division modulation.

228. (Previously Presented) The spread spectrum communications device according to claim 224, wherein the RF wireless communications device performs frequency hopping.

229. (Previously Presented) The spread spectrum communications device according to claim 228, wherein the RF wireless communications device performs orthogonal frequency division modulation.

230. (Previously Presented) The spread spectrum communications device according to claim 224, wherein the RF wireless communications device supports a plurality of spread spectrum modulation techniques.

231. (Previously Presented) The spread spectrum wireless communications device according to claim 224, wherein the integrated circuit is part of a single integrated circuit chip.

232. (Previously Presented) The spread spectrum wireless communications device according to claim 222, wherein the spread spectrum wireless communications device performs frequency hopping.

233. (Previously Presented) The spread spectrum wireless communications device according to claim 222, wherein the spread spectrum wireless communications device performs direct sequence spread spectrum modulation.

234. (Previously Presented) The spread spectrum wireless communications device according to claim 222, wherein the spread spectrum wireless communications device supports a plurality of different wireless spread spectrum modulation techniques.

235. (Previously Presented) The spread spectrum wireless communications device according to claim 222, wherein the spread spectrum wireless communications device performs orthogonal frequency division multiplexing.

236. (Previously Presented) The spread spectrum wireless communications device according to claim 222, wherein the spread spectrum wireless communications device supports communications using direct sequence spread spectrum modulation and communications using orthogonal frequency division multiplexing.

237. (Previously Presented) The spread spectrum wireless communications device according to claim 222, wherein the spread spectrum wireless communications device supports communications using frequency hopping and communications using orthogonal frequency division multiplexing.

238. (Currently Amended) The CMOS integrated circuit according to claim ~~164~~ 298, wherein the transmitter is part of a wireless communications device.

239. (Previously Presented) The CMOS integrated circuit according to claim 238, wherein the wireless communications device comprises a radio frequency (RF) wireless communications device.

240. (Previously Presented) The CMOS integrated circuit according to claim 239, wherein the RF wireless communications device performs orthogonal frequency division multiplexing.

241. (Previously Presented) The CMOS integrated circuit according to claim 239, wherein the RF wireless communications device performs direct sequence spread spectrum modulation.

242. (Previously Presented) The CMOS integrated circuit according to claim 241, wherein the RF wireless communications device performs orthogonal frequency division multiplexing.

243. (Previously Presented) The CMOS integrated circuit according to claim 239, wherein the RF wireless communications device performs frequency hopping.

244. (Previously Presented) The CMOS integrated circuit according to claim 243, wherein the RF wireless communications device performs orthogonal frequency division multiplexing.

245. (Previously Presented) The CMOS integrated circuit according to claim 238, wherein the wireless communications device comprises an RF spread spectrum wireless communications device.

246. (Previously Presented) The CMOS integrated circuit according to claim 238, wherein the CMOS integrated circuit is part of a single integrated circuit chip.

247. (Previously Presented) The CMOS integrated circuit according to claim 246, wherein the single integrated circuit chip comprises a receiver.

248. (Currently Amended) The transmission system according to claim ~~182~~ 299, wherein the transmitter is part of a wireless communications device.

249. (Previously Presented) The transmission system according to claim 248, wherein the wireless communications device comprises a radio frequency (RF) wireless communications device.

250. (Previously Presented) The transmission system according to claim 249, wherein the RF wireless communications device performs orthogonal frequency division multiplexing.

251. (Previously Presented) The transmission system according to claim 249, wherein the RF wireless communications device performs direct sequence spread spectrum modulation.

252. (Previously Presented) The transmission system according to claim 251, wherein the RF wireless communications device performs orthogonal frequency division multiplexing.

253. (Previously Presented) The transmission system according to claim 249, wherein the RF wireless communications device performs frequency hopping.

254. (Previously Presented) The transmission system according to claim 253, wherein the RF wireless communications device performs orthogonal frequency division multiplexing.

255. (Previously Presented) The transmission system according to claim 248, wherein the wireless communications device comprises an RF spread spectrum wireless communications device.

256. (Previously Presented) The transmission system according to claim 249, wherein the transmitter is part of a single integrated circuit chip.

257. (Previously Presented) The transmission system according to claim 256, wherein the single integrated circuit chip comprises a receiver of the wireless communications device.

258. (Previously Presented) The transmission system according to claim 248,

wherein the wireless communications device comprises a spread spectrum wireless communications device,

wherein the transmitter is part of a single integrated circuit chip, and

wherein the single integrated circuit chip is part of the spread spectrum wireless communications device.

259. (Previously Presented) The transmission system according to claim 258, wherein the single integrated circuit chip comprises a receiver of the spread spectrum wireless communications device.

260. (Previously Presented) The CMOS transmitter system according to claim 199, wherein the CMOS transmitter system is part of a wireless communications device.

261. (Previously Presented) The CMOS transmitter system according to claim 260, wherein the wireless communications device comprises a radio frequency (RF) wireless communications device.

262. (Previously Presented) The CMOS transmitter system according to claim 261, wherein the RF wireless communications device performs orthogonal frequency division multiplexing.

263. (Previously Presented) The CMOS transmitter system according to claim 261, wherein the RF wireless communications device performs direct sequence spread spectrum modulation.

264. (Previously Presented) The CMOS transmitter system according to claim 263, wherein the RF wireless communications device performs orthogonal frequency division multiplexing.

265. (Previously Presented) The CMOS transmitter system according to claim 261, wherein the RF wireless communications device performs frequency hopping.

266. (Previously Presented) The CMOS transmitter system according to claim 265, wherein the RF wireless communications device performs orthogonal frequency division multiplexing.

267. (Previously Presented) The CMOS transmitter system according to claim 260, wherein the wireless communications device comprises an RF spread spectrum wireless communications device.

268. (Previously Presented) The CMOS transmitter system according to claim 267, wherein the CMOS transmitter system is part of a single integrated circuit chip.

269. (Previously Presented) The CMOS transmitter system according to claim 268, wherein the single integrated circuit chip comprises a receiver of the wireless communications device.

270. (Previously Presented) The transmitter system according to claim 211, wherein the transmitter system is part of a wireless communications device.

271. (Previously Presented) The transmitter system according to claim 270, wherein the wireless communications device comprises a radio frequency (RF) wireless communications device.

272. (Previously Presented) The transmitter system according to claim 271, wherein the RF wireless communications device performs orthogonal frequency division multiplexing.

273. (Previously Presented) The transmitter system according to claim 271, wherein the RF wireless communications device performs direct sequence spread spectrum modulation.

274. (Previously Presented) The transmitter system according to claim 273, wherein the RF wireless communications device performs orthogonal frequency division multiplexing.

275. (Previously Presented) The transmitter system according to claim 271, wherein the RF wireless communications device performs frequency hopping.

276. (Previously Presented) The transmitter system according to claim 275, wherein the RF wireless communications device performs orthogonal frequency division multiplexing.

277. (Previously Presented) The transmitter system according to claim 270, wherein the wireless communications device comprises an RF spread spectrum wireless communications device.

278. (Previously Presented) The transmitter system according to claim 271,

wherein the transmitter system employs complementary metal oxide semiconductor (CMOS) technology, and

wherein the first oscillator means, the mixer means, the filter means, the detector means and the second oscillator means are part of a single integrated circuit chip.

279. (Previously Presented) The transmitter system according to claim 278, wherein the single integrated circuit chip comprises a receiver of the wireless communications device.

280. (Previously Presented) The spread spectrum wireless communications device according to claim 222, wherein the tunable oscillator comprises a voltage controlled oscillator.

281. (Previously Presented) The spread spectrum wireless communications device according to claim 222, wherein the transmitter comprises a bandpass filter that is operatively coupled between the output of the mixer and the first input of the phase detector.

282. (Previously Presented) The spread spectrum wireless communications device according to claim 281, wherein the transmitter comprises a limiter that is operatively coupled between the bandpass filter and the first input of the phase detector.

283. (Previously Presented) The spread spectrum wireless communications device according to claim 222, wherein the transmitter comprises a charge pump that is operatively coupled between the output of the phase detector and the tuning input.

284. (Previously Presented) The spread spectrum wireless communications device according to claim 222, wherein the transmitter comprises a loop filter that is operatively coupled between the output of the phase detector and the tuning input.

285. (Previously Presented) The spread spectrum wireless communications device according to claim 222,

wherein the tunable oscillator comprises a voltage controlled oscillator,

wherein the integrated circuit comprises a bandpass filter, a limiter, a charge pump and a loop filter,

wherein the bandpass filter is operatively coupled to the mixer,

wherein the limiter is operatively coupled between the bandpass filter and the first input of the phase detector,

wherein the charge pump is operatively coupled to the phase detector output, and

wherein the loop filter is operatively coupled between the charge pump and the tuning input.

286. (Previously Presented) The spread spectrum wireless communications device according to claim 222, wherein the mixer comprises a subsampling mixer.

287. (Previously Presented) The spread spectrum wireless communications device according to claim 286,

wherein the mixer comprises a track and hold circuit and a bandpass circuit,

wherein the track and hold circuit is operatively coupled to the first input of the mixer, the second input of the mixer and the output of the mixer, and

wherein the bandpass circuit is operatively coupled to the first input of the mixer and the output of the mixer.

288. (Previously Presented) The spread spectrum wireless communications device according to claim 287, wherein the mixer comprises an input circuit that is disposed between the first input of the mixer and the track and hold circuit.

289. (Previously Presented) The spread spectrum wireless communications device according to claim 287, wherein the mixer comprises a buffer that is disposed between the track and hold circuit and the output of the mixer.

290. (Previously Presented) The spread spectrum wireless communications device according to claim 287,

wherein the bandpass circuit comprises an inductor and a capacitor,

wherein the inductor is operatively coupled to the first input of the mixer, and

wherein the capacitor is operatively coupled to the output of the mixer.

291. (Previously Presented) The spread spectrum wireless communications device according to claim 287,

wherein the track and hold circuit comprises a switch that is disposed between the first input of the mixer and the output of the mixer, and

wherein the switch is controlled by a signal that is applied to the second input of the mixer from the local oscillator.

292. (Previously Presented) The spread spectrum wireless communications device according to claim 291,

wherein the switch comprises a transistor having a gate, a source and a drain,

wherein the gate is operatively coupled to the second input of the mixer,

wherein the source is operatively coupled to the first input of the mixer,

wherein the bandpass circuit comprises a capacitor and an inductor,

wherein the capacitor is operatively coupled to the drain, and

wherein the inductor is operatively coupled to the source.

293. (Previously Presented) The spread spectrum wireless communications device according to claim 292, wherein the capacitor and the inductor cooperate to provide a time constant that is related to a signal frequency that is applied to the first input of the mixer from the tunable oscillator.

294. (Previously Presented) The spread spectrum wireless communications device according to claim 287,

wherein the track and hold circuit comprises a transistor and a current source,

wherein the transistor includes an input node and an output node,

wherein the input node of the transistor is operatively coupled to the first input of the mixer,

wherein the output node of the transistor is operatively coupled to the output of the mixer,

wherein the current source is operatively coupled to the output of the mixer, and

wherein the current source is controlled by a signal that is applied to the second input of the mixer.

295. (Previously Presented) The spread spectrum wireless communications device according to claim 294,

wherein the current source comprises a second transistor having a gate, a drain and a source,

wherein the gate is operatively coupled to the first input of the mixer,

wherein the drain is operatively coupled to the output of the mixer,

wherein the bandpass circuit comprises a capacitor and an inductor,

wherein the capacitor is operatively coupled to the output of the mixer, and

wherein the inductor is operatively coupled to the drain of the second transistor.

296. (Previously Presented) The spread spectrum wireless communications device according to claim 295, wherein the capacitor and the inductor cooperate to provide a time constant that is related to a signal frequency that is applied to the first input of the mixer from the tunable oscillator.

297. (Previously Presented) The spread spectrum wireless communications device according to claim 231, wherein the single integrated circuit chip comprises a receiver of the spread spectrum wireless communications device.

298. (New) A complementary metal oxide semiconductor (CMOS) integrated circuit, comprising:

a transmitter comprising a tunable oscillator having a tuning input, a mixer having a first input coupled the tunable oscillator, a second input, and an output, and a phase detector having a first input coupled to the mixer output, a second input, and an output coupled to the tuning input; and

a local oscillator coupled to the second input of the mixer.

299. (New) A transmission system, comprising:

a transmitter comprising a tunable oscillator having a tuning input, a subsampling mixer having a first input coupled the tunable oscillator, a second input, and an output, and a phase detector having a first input coupled to the mixer output, a second input, and an output coupled to the tuning input; and

a local oscillator coupled to the second input of the mixer.